Xilinx vs Cadence Verilog

1.) Do not use always@(\*), mention the parameters inside the brackets.

2.) Do not use any local parameters or globally parameterised variables. Every size required by the system has to be explicitly defined.

3.) Do not declare output and reg in the same line.

Ex : output reg sum;

Correction : output sum;

reg sum;

4.) Do not use commas inside always@(a , b), it works in ISE but not here. It should be always@(a or b )

5.) Explicitly mention files used in project using [`include “filename.v”] (no brackets)